

**SPECIFICATION**

At page 2, please amend paragraph [0007] as follows:

[0007] FIGS. 1A and 1B ~~is-a~~ are schematic diagrams of one implementation for a high-precision buffer circuit, according to an embodiment of the present invention.

At page 2, please amend paragraph [0011] as follows:

[0011] The embodiments of the present invention and their advantages are best understood by referring to FIGS. 1A through 3 4 of the drawings. Like numerals are used for like and corresponding parts of the various drawings.

At page 5, please amend the first and second paragraphs [0001] as follows:

[~~0001~~19] Alternatively, again assuming an initial steady state for precision buffer circuit 10, a decrease or drop in the input signal  $V_{in}$  at the input terminal (within a given operational range of  $\Delta V/\Delta t$ ) causes the gate-source voltage  $V_{gs}$  of transistor 16 to increase. Accordingly, more current flows through transistor 16. This causes the voltage at the gate of transistor 24 to decrease, and thus, less current flows through transistor 24. This causes the voltage at the output terminal to decrease. Transistor 14 sources current to transistor 18, and thus transistor 18 may have a relatively fixed gate-source voltage  $V_{gs}$ . The decreased voltage at the output terminal causes the source voltage  $V_s$  of transistor 18 to decrease, thereby causing the gate voltages  $V_g$  of transistors 18 and 16 to decrease. This causes the gate-source voltage  $V_{gs}$  of transistor 16 to decrease. Thus, transistors 16 and 18 are brought into balance again for steady state.

[~~0001~~20] In precision buffer circuit 10, in some embodiments, only transistors 16, 18, and 24 are conducting signal currents. The remaining transistors—i.e., transistors 12, 14, ~~18~~, 20,

and 22—are conducting only bias currents, thus operating to provide relatively constant current. As such, precision buffer circuit 10 may provide faster operation within a given operational range of  $\Delta V/\Delta t$  for the input signal  $V_{in}$  compared to previously designed buffer circuits which have more transistors or components providing signal currents.